Formal Verification: An Essential Toolkit for Modern VLSI Design

Erik Seligman, Tom Schubert, M V Achutha Kiran Kumar

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Formal Verification: An Essential Toolkit for Modern VLSI Design presents practical approaches for design and validation, with hands-on advice to help working engineers integrate these techniques into their work. Formal Verification (FV) enables a designer to directly analyze and mathematically explore the quality or other aspects of a Register Transfer Level (RTL) design without using simulations. This can reduce time spent validating designs and more quickly reach a final design for manufacturing. Building on a basic knowledge of SystemVerilog, this book demystifies FV and presents the practical applications that are bringing it into mainstream design and validation processes at Intel and other companies. After reading this book, readers will be prepared to introduce FV in their organization and effectively deploy FV techniques to increase design and validation productivity.

- Learn formal verification algorithms to gain full coverage without exhaustive simulation
- Understand formal verification tools and how they differ from simulation tools
- Create instant test benches to gain insight into how models work and find initial bugs
- Learn from Intel insiders sharing their hard-won knowledge and solutions to complex design problems

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